By substituting Eq. 6 for the $Vg-V_{Tp}$ in Eq. 5 and then substituting Eq. 5 into Eq. 3 and Eq. 4, differential output voltage signal vout can be shown to equal:

$$Vout = \left[\frac{\left(\frac{W}{L}\right)_n \left(\frac{W}{L}\right)_{p2}}{\left(\frac{W}{L}\right)_p \left(\frac{W}{L}\right)_{n2}}\right] * \left[\frac{Vcm - Vc3}{(Vc1 - v_m)Vc2}\right] v_x * v_y$$

As is known in the art, the mobilities μ_p and μ_n are dependent on temperature thus the common mode voltage becomes insensitive to the effects of temperature. Also, any changes of the geometric and process dependent parameters

$$\left(\left(\frac{W}{L}\right), v_T\right)$$

are cancelled. Thus any changes in the common mode voltage Vcm and the biasing voltage level Vg are compensated to correct any variations in the output voltage level vout of the multiplier core due to temperature and voltage. Further, the voltages Vcm, Vc1, Vc2, and Vc3 are constructed to be referenced to the bandgap of silicon to maintain their constant reference.

FIG. 4*c* illustrates the bias circuit of this invention that generates the voltages Vcm, Vc1, Vc2, and Vc3. The input of the bias circuit is a bandgap reference voltage source V_{bg}. The bandgap reference voltage source provides an accurate voltage source referenced to the bandgap voltage of the bulk semiconductor (silicon). The operational amplifier U3 and the MOS transistor M14 are configured such that the voltage V_{bg2} at the source of the MOS transistor M14 is equal to the bandgap reference voltage V_{bg}. This insures that the current I_{ref} flowing through the resistor R_{2a} is constant.

The p-type MOS transistors M10, M11, and M12 are configured and designed as current mirrors. The currents $I_1$and $I_2$are proportional to the current I_{ref} and the relative width-to-length ratios

$$\left(\frac{W}{L}\right)$$

of the p-type MOS transistors M10, M11, and M12.

The n-type MOS transistor M13 has its gate and drain connected to form a diode. The current $I_1$is set such that the drain-to-source voltage is the threshold voltage V_T of the n-type MOS transistor M_{13}. The biasing voltage Vc1 is set at a voltage level of approximately the threshold voltage of the n-type loading device Rn2 plus a constant voltage V_{const} and is equal to approximately 0.6V. The constant voltage V_{const} is equal to the value of the resistor R_3 multiplied by the current I_1.

The common mode voltage V'cm is determined by the current I_2flowing through the resistors R_{2b}, R_3, and R_4 and is equal to:

$$V'cm=I_2(R_{2b}+R_3+R_4).$$

The operational amplifier U4 is configured as a unity gain buffer to prevent additional loading on the current I_2. The output of the operational amplifier U4 performs as the voltage source for the common mode voltage Vcm.

The biasing voltage Vc2 is determined by the current I_2 flowing through the resistor R_{2b} and is found as:

$$Vc2=I_2*R_{2b}.$$

The biasing voltage Vc3 is determined by the current I_2 flowing through the resistor R_{2b} and R_3 and is found as:

$$Vc3=I_2*R_{2b+R3}.$$

To those skilled in the art it will be apparent that a design incorporating n-type MOS load resistors for p-type MOS multipliers can be derived by reversing the roles of the loading devices Rp and Rn in the embodiment as shown in FIG. 4*b* above.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

The invention claimed is:

1. A temperature and process independent analog integrated circuit comprising:

an analog function core responsive to a first differential input signal and a second differential input signal, and having first and second output terminals;

a first loading device having a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal;

a second loading device having a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal; and

a compensation circuit in communication with said first and second control terminals,

wherein said compensation circuit comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals; and

a first differential amplifier having a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

2. The analog integrated circuit of claim 1 wherein said analog function core is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

3. The analog integrated circuit of claim 1 wherein the analog integrated core circuit is a multiplier circuit comprising:

a first current source;

a second current source;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains in communication with the first current source, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains in communication with the second current source, and commonly connected second sources;

a third current source in communication with the commonly connected first sources to form the first output terminal; and

a fourth current source in communication with the commonly connected second sources to form the second output terminal.

4. The analog integrated circuit of claim 1 wherein the first and second loading devices comprise MOS transistors.

5. The analog integrated circuit of claim 1 wherein said compensation circuit further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage source, and an output in communication with the second gate.

6. The analog integrated circuit of claim 5 wherein the first MOS transistor and the first and second loading devices are of the first conductivity type and the second and third MOS transistors are of the second conductivity type.

7. The analog integrated circuit of claim 1 further comprising a biasing circuit to provide the common mode voltage to the first and second loading devices.

8. The analog integrated circuit of claim 5 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide the second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide the third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

9. The analog integrated circuit of claim 7 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

10. A temperature and process independent analog multiplier circuit comprising:

a multiplier core responsive to a first differential input signal and a second differential input signal, and having first and second output terminals;

a first loading device having a first terminal responsive to the first output terminal, a second terminal responsive to a common mode voltage, and a first control terminal;

a second loading device having a third terminal responsive to the second output terminal, a fourth terminal responsive to the common mode voltage, and a second control terminal; and

a compensation circuit in communication with said first and second control terminals,

wherein said compensation circuit comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate in communication with the first and second control terminals; and

a first differential amplifier having a first input in communication with a first bias voltage source, a second input in communication with the first drain, and an output in communication with the first gate and the first and second control terminals.

11. The temperature and process independent analog multiplier circuit of claim 10 wherein the multiplier core comprises:

a first current source;

a second current source;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains in communication with the first current source, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains in communication with the second current source, and commonly connected second sources;

a third current source in communication with the commonly connected first sources to form the first output terminal; and

a fourth current source in communication with the commonly connected second sources to form the second output terminal.

12. The analog multiplier circuit of claim 10 wherein the first and second loading devices comprises MOS transistors.

13. The analog multiplier circuit of claim 10 wherein said compensation circuit further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage source, and an output in communication with the second gate.

14. The analog multiplier circuit of claim 13 wherein the first MOS transistor and the first and second loading devices are of the first conductivity type and the second and third MOS transistors are of the second conductivity type.

15. The analog multiplier circuit of claim 11 further comprising a biasing circuit to provide the common mode voltage to the first and second loading devices.

16. The analog multiplier circuit of claim 13 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide a second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide a third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

17. The analog multiplier circuit of claim 15 wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

18. A temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process, said compensation circuit comprising:

a first MOS transistor having a first source in communication with a common mode voltage, a first drain, and a first gate in communication with the control terminals;

a first differential amplifier having a first input in communication with a first bias voltage, a second input in communication with the first drain, and an output in communication with the control terminals;

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor having a third gate in communication with a second bias voltage, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier having a second input in communication with the third drain and the second source, a third input in communication with a third bias voltage, and an output in communication with the second gate.

19. The temperature and process compensation circuit of claim 18 wherein the first MOS transistor is of the first conductivity type and the second and third MOS transistors are of the second conductivity type.

20. The temperature and process compensation circuit of claim 18 further comprising a biasing circuit to provide the common mode voltage and to provide the first bias voltage, second bias voltage, and third bias voltage to said compensation circuit.

21. The temperature and process compensation circuit of claim 20 further comprising a biasing circuit comprising:

a common mode voltage source to provide the common mode voltage that is referenced to a semiconductor bandgap voltage;

a first bias voltage source to provide a first bias voltage to the first MOS transistor that is referenced to the semiconductor bandgap voltage;

a second bias voltage source to provide a second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage; and

a third bias voltage source to provide a third bias voltage to the third MOS transistor that is referenced to a semiconductor bandgap voltage.

22. A temperature and process independent analog integrated circuit comprising:

analog integrated function means for providing first and second output signals responsive to a first differential input signal and a second differential input;

first loading means for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal;

second loading means for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and

compensation circuit for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

23. The analog integrated circuit of claim 22 wherein said analog integrated function means is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

24. The analog integrated circuit of claim 22 wherein the analog integrated function means is a multiplier circuit comprising:

first current means for supplying a first current;

second current means for supplying a second current;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains responsive to the first current, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains responsive to the second current, and commonly connected second sources;

third current means for supplying a third current and in communication with the commonly connected first sources to form the first output terminal; and

fourth current means for supplying a third current and in communication with the commonly connected second sources to form the second output terminal.

25. The analog integrated circuit of claim 22 wherein the first and second loading means comprise MOS transistors.

26. The analog integrated circuit of claim 22 wherein said compensation means comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, wherein an output of the first differential amplifier means and a signal from the first gate form the compensation control signal.

27. The analog integrated circuit of claim 26 wherein said compensation means further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

28. The analog integrated circuit of claim 27 wherein the first MOS transistor and the first and second loading devices are of the first conductivity type and the second and third MOS transistors are of the second conductivity type.

29. The analog integrated circuit of claim 22 further comprising biasing means to provide the common mode voltage to the first and second loading means.

30. The analog integrated circuit of claim 27 further comprising a biasing circuit comprising:

means for generating the common mode voltage that is referenced to a semiconductor bandgap voltage;

means for providing a first bias voltage that is referenced to the semiconductor bandgap voltage;

means for providing a second bias voltage that is referenced to a semiconductor bandgap voltage; and

means for providing a third bias voltage that is referenced to a semiconductor bandgap voltage.

31. The analog integrated circuit of claim **29** wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

32. A temperature and process independent analog multiplier circuit comprising:

multiplier means for multiplying a first differential input signal and a second differential input to provide first and second output signals;

first loading means for providing an output voltage in response to the first output signal, a common mode voltage signal, and a compensation control signal;

second loading means for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and

compensation circuit for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

33. The temperature and process independent analog multiplier circuit of claim **32** wherein the multiplier means comprises:

first current means for supplying a first current;

second current means for supplying a second current;

a first pair of first and second MOS transistors arranged in parallel having a gate of the first MOS transistor in communication with a first terminal of the first differential input signal, a gate of the second MOS transistor in communication with a second terminal of the first differential input signal, commonly connected first drains responsive to the first current, and commonly connected first sources;

a second pair of third and fourth MOS transistors arranged in parallel having a gate of the third MOS transistor in communication with a first terminal of the second differential input signal, a gate of the fourth MOS transistor in communication with a second terminal of the second differential input signal, commonly connected second drains responsive to the second current, and commonly connected second sources;

third current means for supplying a third current and in communication with the commonly connected first sources to form the first output terminal; and

fourth current means for supplying a third current and in communication with the commonly connected second sources to form the second output terminal.

34. The temperature and process independent analog multiplier circuit of claim **32** wherein the first and second loading devices comprises MOS transistors.

35. The temperature and process independent analog multiplier circuit of claim **32** wherein said compensation means comprises:

a first MOS transistor having a first source in communication with the common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first differential amplifier means and a signal from the first gate form the compensation control signal.

36. The temperature and process independent analog multiplier circuit of claim **35** wherein said compensation means further comprises:

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

37. The temperature and process independent analog multiplier circuit of claim **32** wherein the first MOS transistor and the first and second loading devices are of the first conductivity type and the second and third MOS transistors are of the second conductivity type.

38. The temperature and process independent analog multiplier circuit of claim **35** further comprising biasing means for providing a common mode voltage to the first and second loading.

39. The temperature and process independent analog multiplier circuit of claim **37** further comprising biasing means comprising:

means to generate the common mode voltage that is referenced to a semiconductor bandgap voltage;

means for providing a first bias voltage that is referenced to the semiconductor bandgap voltage;

means for providing a second bias voltage that is referenced to a semiconductor bandgap voltage; and

means for providing a third bias voltage that is referenced to a semiconductor bandgap voltage.

40. The analog integrated circuit of claim **38** wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

41. A temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process, said compensation circuit comprising:

a first MOS transistor having a first source in communication with a common mode voltage, a first drain, and a first gate; and

first differential amplifier means for differentially amplifying a first bias voltage source and a signal from the first drain, and an output, wherein the output of the first differential amplifier means and a signal from the first gate form a compensation control signal;

a second MOS transistor having a second gate, a second drain in communication with the first drain and a second source;

a third MOS transistor in communication with a second bias voltage source, a third source in communication with a reference point, and a third drain in communication with the second source; and

a second differential amplifier means for amplifying as a first input the third drain and the second source, and as a second input a third bias voltage source, and to provide output to the second gate.

42. The compensation circuit of claim 41 wherein the first MOS transistor is of the first conductivity type and the second and third MOS transistors are of the second conductivity type.

43. The compensation circuit of claim 41 further comprising biasing means to provide the common mode voltage and to provide the first bias voltage source, second bias voltage source, and third bias voltage source to said compensation circuit.

44. The compensation circuit of claim 43 wherein said biasing means comprises:

means to generate the common mode voltage that is referenced to a semiconductor bandgap voltage;

means to generate a first bias voltage that is referenced to the semiconductor bandgap voltage;

means to generate the second bias voltage circuit that is referenced to the semiconductor bandgap voltage; and

means to generate the third bias voltage that is referenced to the semiconductor bandgap voltage.

* * * * *